PCF85063TP

Tiny Real-Time Clock/calendar

Rev. 2 — 15 April 2013 **Product data sheet**

1. General description

The PCF85063TP is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power consumption. An offset register allows fine-tuning of the clock. All addresses and data are transferred serially via the two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbit/s. The register address is incremented automatically after each written or read data byte.

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Clock operating voltage: 0.9 V to 5.5 V
- Low current: typical 0.22 μA at V_{DD} = 3.3 V and T_{amb} = 25 °C
- 400 kHz two-line I^2C-bus interface (at V_{DD} = 1.8 V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz, and 1 Hz)
- Selectable integrated oscillator load capacitors for C_L = 7 pF or C_L = 12.5 pF
- Minute and half minute interrupt
- Internal Power-On Reset (POR)
- Programmable offset register for frequency adjustment

3. Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment
- Battery powered devices

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF85063TP	HWSON8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.75 mm	SOT1069-2

4.1 Ordering options

Table 2. Ordering options

Product type number	IC revision	Sales item (12NC)	Delivery form
PCF85063TP/1	1	935297365118	tape and reel, 13 inch

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCF85063TP/1	063

6. Block diagram

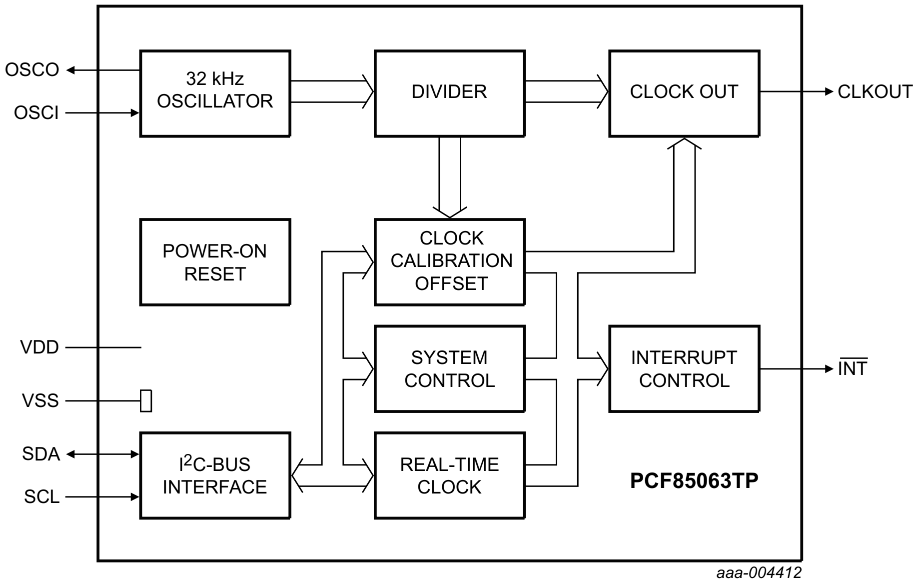
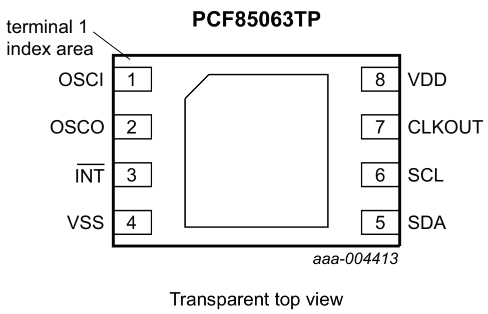


Fig 1. Block diagram of PCF85063TP

7. Pinning information

7.1 Pinning



For mechanical details, see Figure 27.

Fig 2. Pin configuration for HWSON8 (PCF85063TP)

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
OSCI	1	input	oscillator input
OSCO	2	output	oscillator output
$\overline{INT}$	3	output	interrupt output (open-drain)
VSS	4[1]	supply	ground supply voltage
SDA	5	input/output	serial data line
SCL	6	input	serial clock input
CLKOUT	7	output	clock output (push-pull)
VDD	8	supply	supply voltage

[1] The die paddle (exposed pad) is connected to V_{SS} and should be electrically isolated.

8. Functional description

The PCF85063TP contains 11 8-bit registers with an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calender, and an I^2C-bus interface with a maximum data rate of 400 kbit/s.

The built-in address register will increment automatically after each read or write of a data byte up to the register 0Ah. After register 0Ah, the auto-incrementing will wrap around to address 00h (see Figure 3).

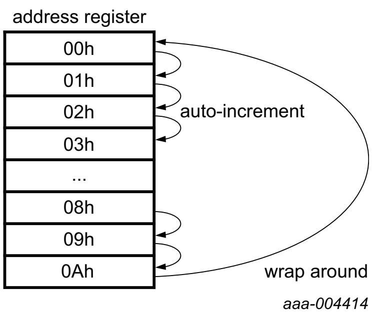


Fig 3. Handling address registers

All 11 registers (see Table 5) are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and status register. The register at address 02h is an offset register allowing the fine-tuning of the clock; and at 03h is a free RAM byte. The addresses 04h through 0Ah are used as counters for the clock function (seconds up to years counters).

The Seconds, Minutes, Hours, Days, Months, and Years registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

8.1 Registers organization

Table 5. Registers overview

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 8 on page 9.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Control and status registers										
00h	Control_1	EXT_TEST	-	STOP	SR	-	CIE	12_24	CAP_SEL	Section 8.2.1
01h	Control_2	-	-	MI	HMI	TF	COF[2:0]			Section 8.2.2
02h	Offset	MODE	OFFSET[6:0]							Section 8.2.3
03h	RAM_byte	B[7:0]								Section 8.2.4
Time and date registers										
04h	Seconds	OS	SECONDS (0 to 59)							Section 8.3.1
05h	Minutes	-	MINUTES (0 to 59)							Section 8.3.2
06h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 hour mode					Section 8.3.3
				HOURS (0 to 23) in 24 hour mode						
07h	Days	-	-	DAYS (1 to 31)						Section 8.3.4
08h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			Section 8.3.5
09h	Months	-	-	-	MONTHS (1 to 12)					Section 8.3.6
0Ah	Years	YEARS (0 to 99)								Section 8.3.7

8.2 Control registers

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST		**external clock test mode**	Section 8.2.1.1
		0[1]	normal mode	
		1	external clock test mode	
6	-	0	unused	-
5	STOP		**STOP bit**	Section 8.2.1.2
		0[1]	RTC clock runs	
		1	RTC clock is stopped; all RTC divider chain flip-flops are asynchronously set logic 0	
4	SR		**software reset**	Section 8.2.1.3
		0[1]	no software reset	
		1	initiate software reset[2]; this bit always returns a 0 when read	
3	-	0	unused	-
2	CIE		**correction interrupt enable**	Section 8.2.3
		0[1]	no correction interrupt generated	
		1	interrupt pulses are generated at every correction cycle	
1	12_24		**12 or 24 hour mode**	Section 8.3.3
		0[1]	24 hour mode is selected	
		1	12 hour mode is selected	
0	CAP_SEL		**internal oscillator capacitor selection** for quartz crystals with a corresponding load capacitance	-
		0[1]	7 pF	
		1	12.5 pF	

[1] Default value.

[2] For a software reset, 01011000 (58h) must be sent to register Control_1 (see Section 8.2.1.3).

8.2.1.1 EXT_TEST: external clock test mode

A test mode is available which allows for on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST in register Control_1. Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal with the signal applied to pin CLKOUT.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1)
2. Set STOP (register Control_1, bit STOP = 1)
3. Clear STOP (register Control_1, bit STOP = 0)
4. Set time registers to desired value
5. Apply 32 clock pulses to pin CLKOUT
6. Read time registers to see the first change
7. Apply 64 clock pulses to pin CLKOUT
8. Read time registers to see the second change

Repeat 7 and 8 for additional increments.

8.2.1.2 STOP: STOP bit function

The function of the STOP bit (see Figure 4) is to allow for accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks are generated. It also stops the output of clock frequencies lower than 8 kHz on pin CLKOUT.

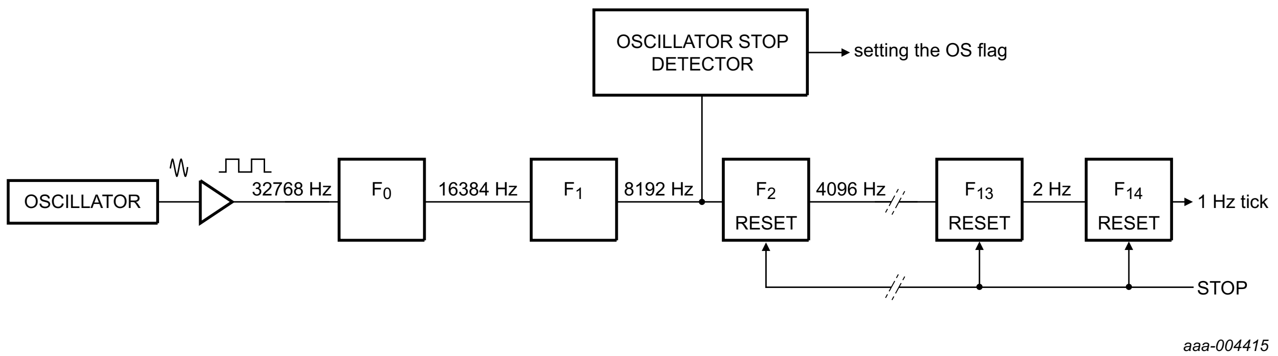
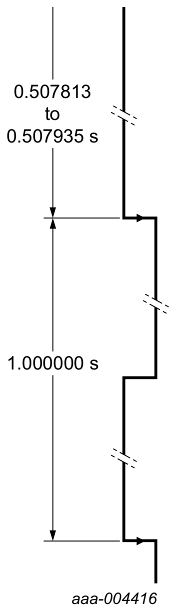


Fig 4. STOP bit functional diagram

The time circuits can then be set and do not increment until the STOP bit is released (see Figure 5 and Table 7).

Table 7. First increment of time circuits after STOP bit release

Bit STOP	Prescaler bits F_0F_1-F_2 to F_{14} [1]	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP bit is activated by user. F_0F_1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	:
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F_{14} increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

The lower two stages of the prescaler (F_0 and F_1) are not reset. And because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle (see Figure 5).

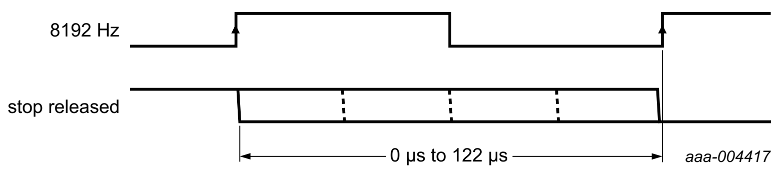


Fig 5. STOP bit release timing

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see Table 7) and the unknown state of the 32 kHz clock.

8.2.1.3 Software reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. Software reset command means setting bits 6, 4, and 3 in register Control_1 (00h) logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see Figure 6.

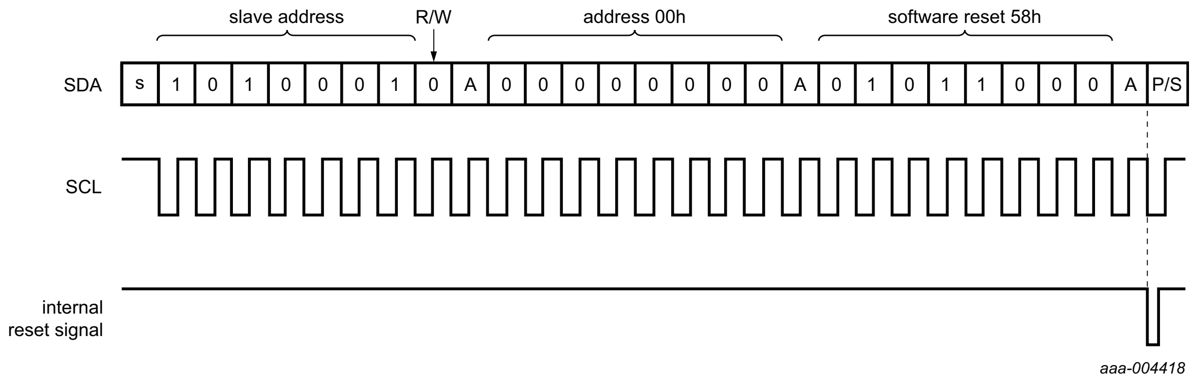


Fig 6. Software reset command

In reset state all registers are set according to Table 8 and the address pointer returns to address 00h.

Table 8. Register reset values

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	0	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Offset	0	0	0	0	0	0	0	0
03h	RAM_byte	0	0	0	0	0	0	0	0
04h	Seconds	1	0	0	0	0	0	0	0
05h	Minutes	0	0	0	0	0	0	0	0
06h	Hours	0	0	0	0	0	0	0	0
07h	Days	0	0	0	0	0	0	0	1
08h	Weekdays	0	0	0	0	0	1	1	0
09h	Months	0	0	0	0	0	0	0	1
0Ah	Years	0	0	0	0	0	0	0	0

The PCF85063TP resets to:

Time — 00:00:00

Date — 20000101

Weekday — Saturday

8.2.2 Register Control_2

Table 9. Control_2 - control and status register 2 (address 01h) bit description

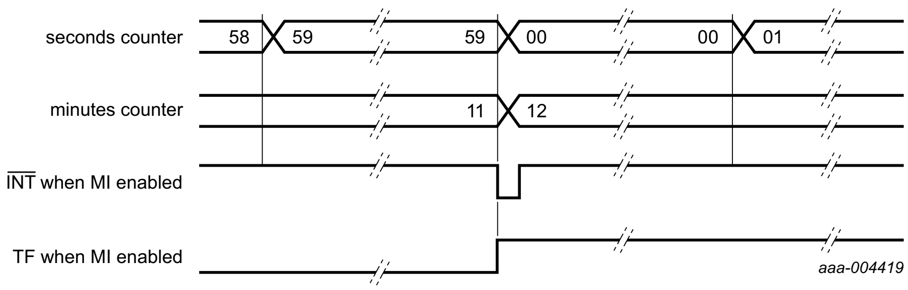
Bit	Symbol	Value	Description
7 to 6	-	00	unused
5	MI		**minute interrupt**
		0[1]	disabled
		1	enabled
4	HMI		**half minute interrupt**
		0[1]	disabled
		1	enabled
3	TF		**timer flag**
		0[1]	no timer interrupt generated
		1	flag set when timer interrupt generated
2 to 0	COF[2:0]	see Table 11	**CLKOUT control**

[1] Default value.

8.2.2.1 MI and HMI: minute and half minute interrupt

The minute interrupt (bit MI) and half minute interrupt (bit HMI) are pre-defined timers for generating interrupt pulses on pin $\overline{\text{INT}}$; see Figure 7. The timers are running in sync with the seconds counter (see Table 19 on page 16).

When starting MI, the first interrupt will be generated after 1 second to 59 seconds. When starting HMI, the first interrupt will be generated after 1 second to 29 seconds. Subsequent periods do not have such a delay. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a half minute interrupt is not distinguishable.



In this example, the TF flag is not cleared after an interrupt.

Fig 7. $\overline{\text{INT}}$ example for MI

Table 10. Effect of bits MI and HMI on $\overline{\text{INT}}$ generation

Minute interrupt (bit MI)	Half minute interrupt (bit HMI)	Result
0	0	no interrupt generated
1	0	an interrupt every minute
0	1	an interrupt every 30 s
1	1	an interrupt every 30 s

The duration of the timer is affected by the register Offset (see Section 8.2.3). Only when OFFSET[6:0] has the value 00h the periods are consistent.

8.2.2.2 TF: timer flag

The timer flag (bit TF) is set logic 1 on the first trigger of MI or HMI and remains set until it is cleared by command.

8.2.2.3 COF[2:0]: Clock output frequency

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Control_2. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is a push-pull output and enabled at power-on. CLKOUT can be disabled by setting COF[2:0] to 111. When disabled, the CLKOUT is LOW.

The duty cycle of the selected clock is not controlled but due to the nature of the clock generation, all clock frequencies except 32.768 kHz have a duty cycle of 50 : 50.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped. For more details of the STOP bit function, see Section 8.2.1.2.

Table 11. CLKOUT frequency selection

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]	Effect of STOP bit
000[2]	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW
101	1024	50 : 50	CLKOUT = LOW
110	1[3]	50 : 50	CLKOUT = LOW
111	CLKOUT = LOW	-	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] 1 Hz clock pulses are affected by offset correction pulses.

8.2.3 Register Offset

The PCF85063TP incorporates an offset register (address 02h) which can be used to implement several functions, such as:

- Accuracy tuning
- Aging adjustment
- Temperature compensation

Table 12. Offset - offset register (address 02h) bit description

Bit	Symbol	Value	Description
7	MODE		**offset mode**
		0[1]	normal mode: offset is made once every two hours
		1	course mode: offset is made every 4 minutes
6 to 0	OFFSET[6:0]	see Table 13	**offset value**

[1] Default value.

For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The values of 4.34 ppm and 4.069 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to –64 LSB.

Table 13. Offset values

OFFSET[6:0]	Offset value in decimal	Offset value in ppm	
		Normal mode MODE = 0	Fast mode MODE = 1
0111111	+63	+273.420	+256.347
0111110	+62	+269.080	+252.278
:	:	:	:
0000010	+2	+8.680	+8.138
0000001	+1	+4.340	+4.069
0000000[1]	0	0[1]	0[1]
1111111	–1	–4.340	–4.069
1111110	–2	–8.680	–8.138
:	:	:	:
1000001	–63	–273.420	–256.347
1000000	–64	–277.760	–260.416

[1] Default value.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second but not by changing the oscillator frequency.

It is possible to monitor when correction pulses are applied. To enable correction interrupt generation, bit CIE (register Control_1) has to be set logic 1. At every correction cycle a pulse is generated on pin $\overline{\text{INT}}$. The pulse width depends on the correction mode. If multiple correction pulses are applied, an interrupt pulse is generated for each correction pulse applied.

8.2.3.1 Correction when MODE = 0

The correction is triggered once every two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 14. Correction pulses for MODE = 0

Correction value	Update every nth hour	Minute	Correction pulses on $\overline{INT}$ per minute[1]
+1 or –1	2	00	1
+2 or –2	2	00 and 01	1
+3 or –3	2	00, 01, and 02	1
:	:	:	:
+59 or –59	2	00 to 58	1
+60 or –60	2	00 to 59	1
+61 or –61	2	00 to 59	1
	2nd and next hour	00	1
+62 or –62	2	00 to 59	1
	2nd and next hour	00 and 01	1
+63 or –63	02	00 to 59	1
	2nd and next hour	00, 01, and 02	1
–64	02	00 to 59	1
	2nd and next hour	00, 01, 02, and 03	1

[1] The correction pulses on pin $\overline{INT}$ are $^{1}\!/_{64}$ s wide.

In MODE = 0, any timer or clock output using a frequency below 64 Hz is affected by the clock correction (see Table 15).

Table 15. Effect of correction pulses on frequencies for MODE = 0

Frequency (Hz)	Effect of correction
CLKOUT	
32768	no effect
16384	no effect
8192	no effect
4096	no effect
2048	no effect
1024	no effect
1	affected
Timer source clock	
4096	no effect
64	no effect
1	affected
$^{1}\!/_{60}$	affected

8.2.3.2 Correction when MODE = 1

The correction is triggered once every four minutes and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Table 16. Correction pulses for MODE = 1

Correction value	Update every nth minute	Second	Correction pulses on $\overline{INT}$ per second[1]
+1 or –1	2	00	1
+2 or –2	2	00 and 01	1
+3 or –3	2	00, 01, and 02	1
:	:	:	:
+59 or –59	2	00 to 58	1
+60 or –60	2	00 to 59	1
+61 or –61	2	00 to 58	1
	2	59	2
+62 or –62	2	00 to 58	1
	2	59	3
+63 or –63	2	00 to 58	1
	2	59	4
–64	2	00 to 58	1
	2	59	5

[1] The correction pulses on pin $\overline{INT}$ are $^1\!/_{1024}$ s wide. For multiple pulses, they are repeated at an interval of $^1\!/_{512}$ s.

In MODE = 1, any timer source clock using a frequency below 1.024 kHz is also affected by the clock correction (see Table 17).

Table 17. Effect of correction pulses on frequencies for MODE = 1

Frequency (Hz)	Effect of correction
CLKOUT	
32768	no effect
16384	no effect
8192	no effect
4096	no effect
2048	no effect
1024	no effect
1	affected
Timer source clock	
4096	no effect
64	affected
1	affected
$^1\!/_{60}$	affected

8.2.3.3 Offset calibration workflow

The calibration offset has to be calculated based on the time. Figure 8 shows the workflow how the offset register values can be calculated:

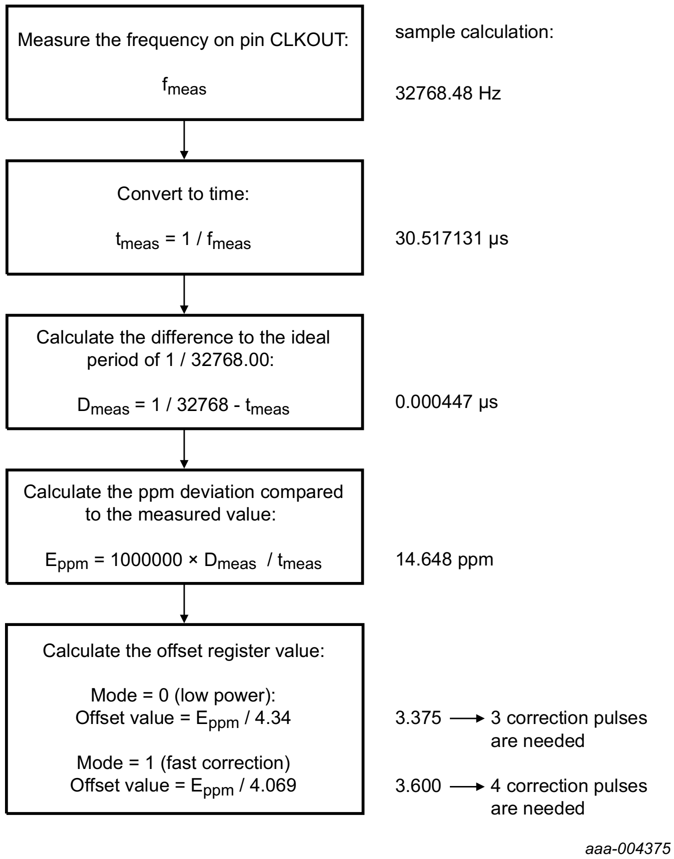
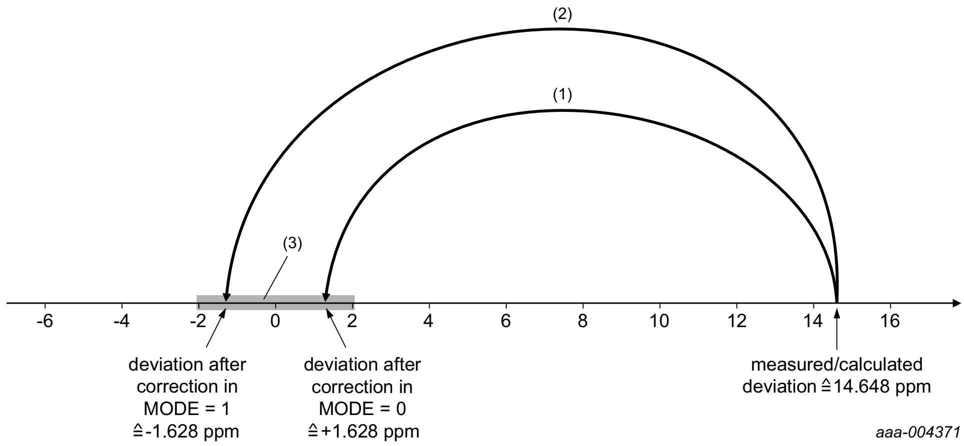


Fig 8. Offset calibration calculation workflow



With the offset calibration an accuracy of ±2 ppm (0.5 × offset per LSB) can be reached (see Table 13).

±1 ppm corresponds to a time deviation of 0.0864 seconds per day.

(1) 3 correction pulses in MODE = 0 correspond to −13.02 ppm.

(2) 4 correction pulses in MODE = 1 correspond to −16.276 ppm.

(3) Reachable accuracy zone.

Fig 9. Result of offset calibration

8.2.4 Register RAM_byte

The PCF85063TP provides a free RAM byte, which can be used for any purpose, for example, status byte of the system.

Table 18. RAM_byte - 8-bit RAM register (address 03h) bit description

Bit	Symbol	Value	Description
7 to 0	B[7:0]	00000000[1] to 11111111	**RAM content**

[1] Default value.

8.3 Time and date registers

Most of the registers are coded in the BCD format to simplify application use.

8.3.1 Register Seconds

Table 19. Seconds - seconds register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7	OS			**oscillator stop**
		0	-	clock integrity is guaranteed
		1[1]	-	clock integrity is not guaranteed; oscillator has stopped or has been interrupted
6 to 4	SECONDS	0[1] to 5	ten's place	**actual seconds** coded in BCD format, see Table 20
3 to 0		0[1] to 9	unit place	

[1] Default value.

Table 20. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00[1]	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

[1] Default value.

8.3.1.1 OS: Oscillator stop

When the oscillator of the PCF85063TP is stopped, the OS flag is set. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature, and supply voltage.

The flag remains set until cleared by command (see Figure 10). If the flag cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

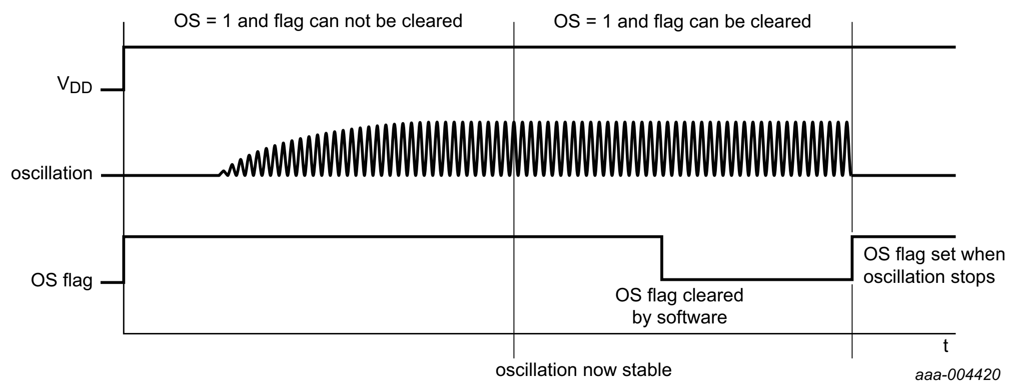


Fig 10. OS flag

8.3.2 Register Minutes

Table 21. Minutes - minutes register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7	-	0	-	unused
6 to 4	MINUTES	0[1] to 5	ten's place	**actual minutes** coded in BCD format
3 to 0		0[1] to 9	unit place	

[1] Default value.

8.3.3 Register Hours

Table 22. Hours - hours register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	00	-	unused
12 hour mode[1]				
5	AMPM			**AM/PM indicator**
		0[2]	-	AM
		1	-	PM
4	HOURS	0[2] to 1	ten's place	**actual hours in 12 hour mode** coded in BCD format
3 to 0		0[2] to 9	unit place	
24 hour mode[1]				
5 to 4	HOURS	0[2] to 2	ten's place	**actual hours in 24 hour mode** coded in BCD format
3 to 0		0[2] to 9	unit place	

[1] Hour mode is set by the 12_24 bit in register Control_1.

[2] Default value.

8.3.4 Register Days

Table 23. Days - days register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	00	-	unused
5 to 4	DAYS[1]	0[2] to 3	ten's place	**actual day** coded in BCD format
3 to 0		0[3] to 9	unit place	

[1] If the year counter contains a value, which is exactly divisible by 4 (including the year 00), the PCF85063TP compensates for leap years by adding a 29th day to February.

[2] Default value.

[3] Default value is 1.

8.3.5 Register Weekdays

Table 24. Weekdays - weekdays register (address 08h) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	unused
2 to 0	WEEKDAYS	0 to 6	**actual weekday** values, see Table 25

Table 25. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday[2]	1	1	0

[1] Definition may be reassigned by the user.

[2] Default value.

8.3.6 Register Months

Table 26. Months - months register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7 to 5	-	000	-	unused
4	MONTHS	0 to 1	ten's place	**actual month** coded in BCD format, see Table 27
3 to 0		0 to 9	unit place	

Table 27. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January[1]	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

[1] Default value.

8.3.7 Register Years

Table 28. Years - years register (0Ah) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0[1] to 9	ten's place	**actual year** coded in BCD format
3 to 0		0[1] to 9	unit place	

[1] Default value.

8.4 Setting and reading the time

Figure 11 shows the data flow and data dependencies starting from the 1 Hz clock tick.

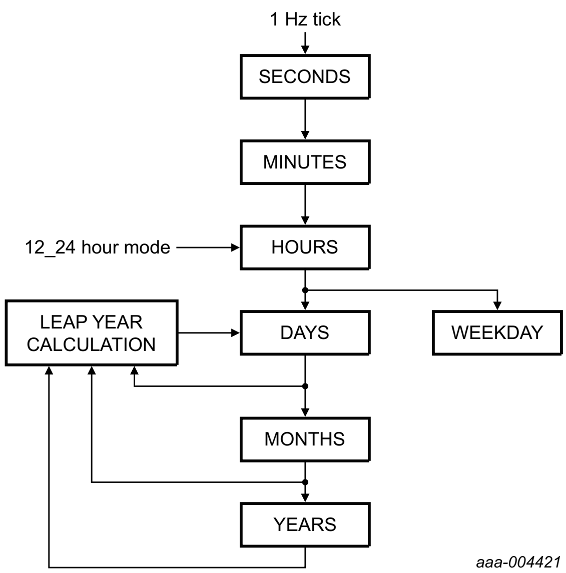


Fig 11. Data flow for the time function

During read/write operations, the time counting circuits (memory locations 04h through 0Ah) are blocked.

The blocking prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 12).

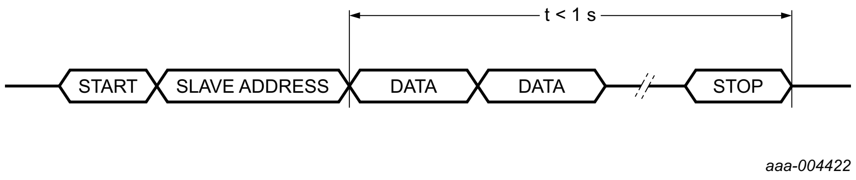


Fig 12. Access time for read/write operations

Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address (see Table 29 on page 24) for write (A2h)
2. Set the address pointer to 4 (Seconds) by sending 04h
3. Send a RESTART condition or STOP followed by START
4. Send the slave address for read (A3h)
5. Read Seconds
6. Read Minutes
7. Read Hours
8. Read Days
9. Read Weekdays
10. Read Months
11. Read Years
12. Send a STOP condition

9. Characteristics of the I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signal (see Figure 13).

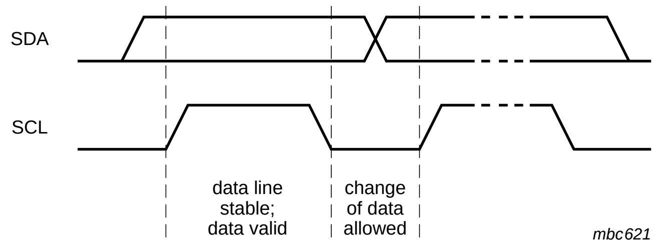


Fig 13. Bit transfer

9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 14).

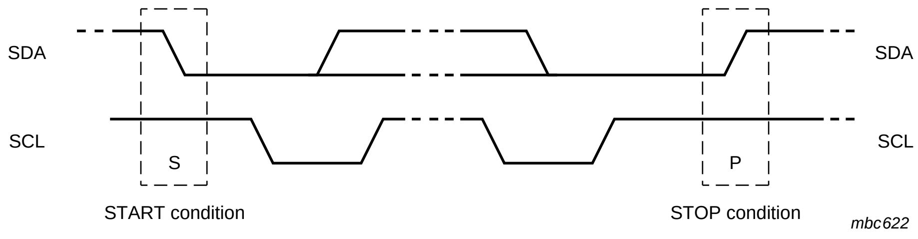


Fig 14. Definition of START and STOP conditions

9.3 System configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see Figure 15).

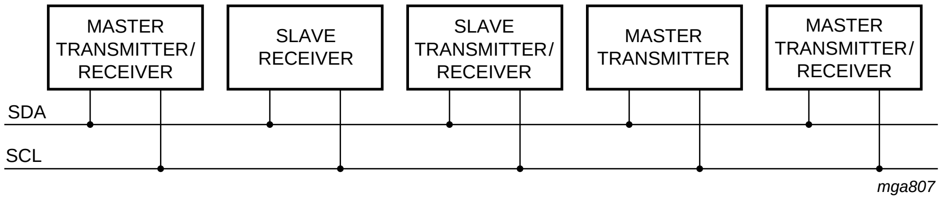


Fig 15. System configuration

9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I^{2}C-bus is shown in Figure 16.

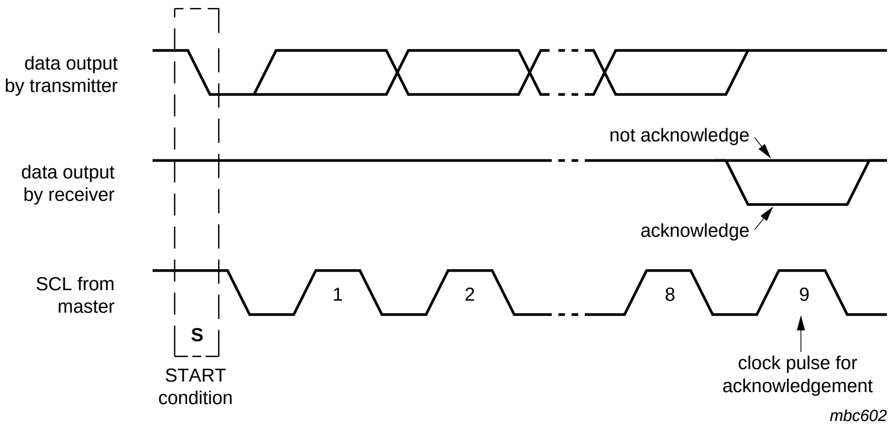


Fig 16. Acknowledgement on the I^{2}C-bus

9.5 I²C-bus protocol

9.5.1 Addressing

One I²C-bus slave address (1010001) is reserved for the PCF85063TP. The entire I²C-bus slave address byte is shown in Table 29.

Table 29. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
	1	0	1	0	0	0	1	$R/\overline{W}$

After a START condition, the I²C slave address has to be sent to the PCF85063TP device.

The $R/\overline{W}$ bit defines the direction of the following single or multiple byte data transfer ($R/\overline{W}$ = 0 for writing, $R/\overline{W}$ = 1 for reading). For the format and the timing of the START condition (S), the STOP condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics (see Ref. 12 "UM10204"). In the write mode, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

9.5.2 Clock and calendar READ or WRITE cycles

The I²C-bus configuration for the different PCF85063TP READ and WRITE cycles is shown in Figure 17 and Figure 18. The register address is a 4-bit value that defines which register will be accessed next. The upper 4 bits of the register address are not used.

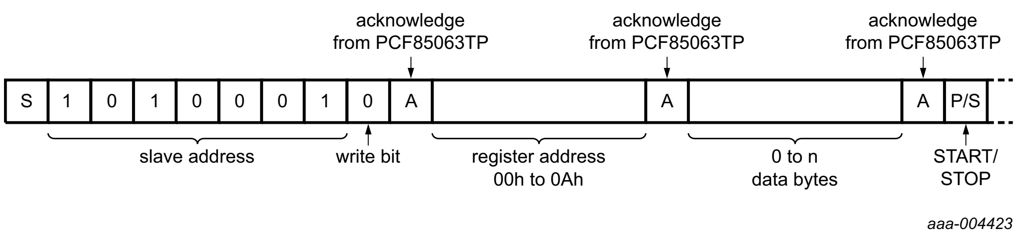
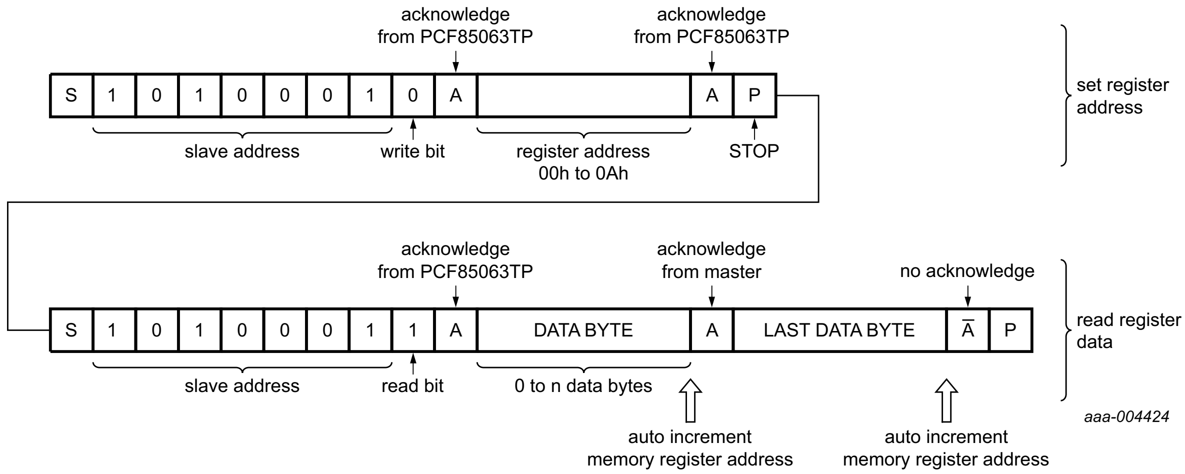


Fig 17. Master transmits to slave receiver (WRITE mode)



For multimaster configurations and to fasten the communication, the STOP-START sequence can be replaced by a repeated START (Sr).

Fig 18. Master reads after setting register address (WRITE register address; READ data)

10. Internal circuitry

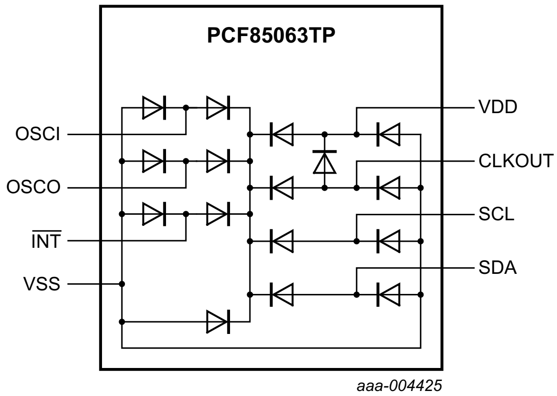


Fig 19. Device diode protection diagram of PCF85063TP

11. Limiting values

Table 30. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
I_{DD}	supply current			–50	+50	mA
V_I	input voltage	on pins SCL, SDA, OSCI		–0.5	+6.5	V
V_O	output voltage			–0.5	+6.5	V
I_I	input current	at any input		–10	+10	mA
I_O	output current	at any output		–10	+10	mA
P_{tot}	total power dissipation			-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±5000	V
		CDM	[2]	-	±1500	V
I_{lu}	latch-up current		[3]	-	200	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 7 “JESD22-A114”.

[2] Pass level; Charged-Device Model (CDM), according to Ref. 8 “JESD22-C101”.

[3] Pass level; latch-up testing, according to Ref. 9 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 13 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

12. Characteristics

Table 31. Static characteristics

V_{DD} = 0.9 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	interface inactive; f_{SCL} = 0 Hz	[1]	0.9	-	5.5	V
		interface active; f_{SCL} = 400 kHz	[1]	1.8	-	5.5	V
I_{DD}	supply current	V_{DD} = 3.3 V	[2]				
		interface inactive; f_{SCL} = 0 Hz					
		T_{amb} = 25 °C		-	220	450	nA
		T_{amb} = 50 °C	[3]	-	250	500	nA
		T_{amb} = 85 °C		-	470	600	nA
		interface active; f_{SCL} = 400 kHz		-	18	50	μA
Inputs[4]							
V_I	input voltage			V_{SS}	-	5.5	V
V_{IL}	LOW-level input voltage			V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	V_{DD}	V
I_{LI}	input leakage current	V_I = V_{SS} or V_{DD}		-	0	-	μA
		post ESD event		−0.15	-	+0.15	μA
C_i	input capacitance		[5]	-	-	7	pF
Outputs							
V_{OH}	HIGH-level output voltage	on pin CLKOUT		$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	on pins SDA, $\overline{INT}$, CLKOUT		V_{SS}	-	$0.2V_{DD}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 2.9 V; V_{DD} = 3.3 V; on pin CLKOUT		1	3	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 3.3 V					
		on pin SDA		3	8.5	-	mA
		on pin $\overline{INT}$		2	6	-	mA
		on pin CLKOUT		1	3	-	mA

Table 31. Static characteristics *...continued*

V_{DD} = 0.9 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	ΔV_{DD} = 200 mV; T_{amb} = 25 °C	-	0.075	-	ppm
$C_{L(itg)}$	integrated load capacitance	on pins OSCO, OSCI [6]				
		C_L = 7 pF	4.2	7	9.8	pF
		C_L = 12.5 pF	7.5	12.5	17.5	pF
R_s	series resistance		-	-	100	kΩ

[1] For reliable oscillator start-up at power-on: $V_{DD(po)min} = V_{DD(min)} + 0.3$ V.

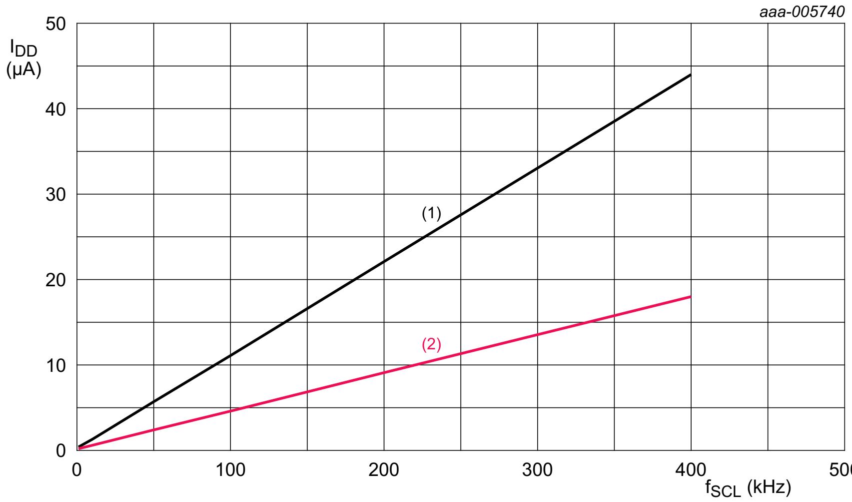
[2] Timer source clock = $^1/_{60}$ Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.

[3] Tested on sample basis.

[4] The I²C-bus interface of PCF85063TP is 5 V tolerant.

[5] Implicit by design.

[6] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

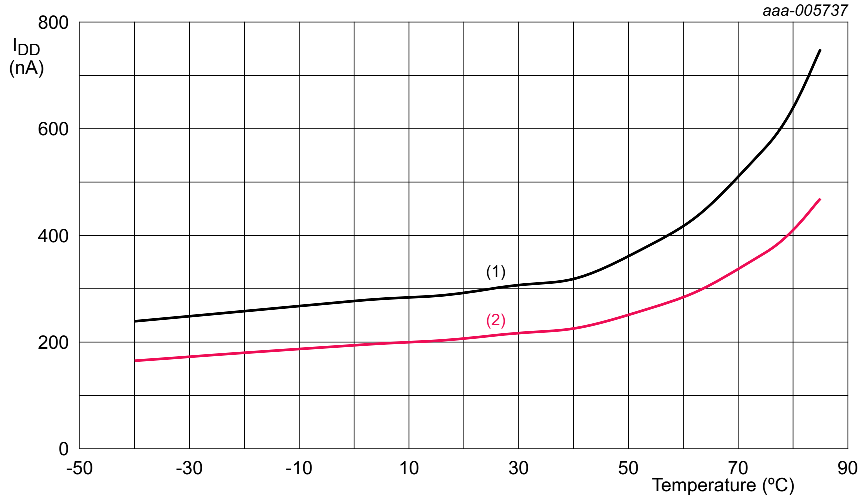


T_{amb} = 25 °C; CLKOUT disabled.

(1) V_{DD} = 5.0 V.

(2) V_{DD} = 3.3 V.

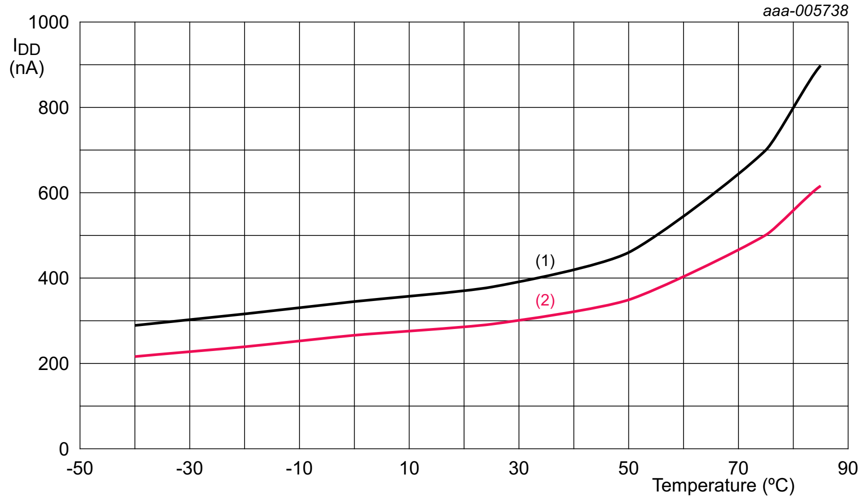
Fig 20. Typical I_{DD} with respect to f_{SCL}



$C_{L(itg)}$ = 7 pF; CLKOUT disabled.

(1) V_{DD} = 5.5 V.

(2) V_{DD} = 3.3 V.



$C_{L(itg)}$ = 12.5 pF; CLKOUT disabled.

(1) V_{DD} = 5.5 V.

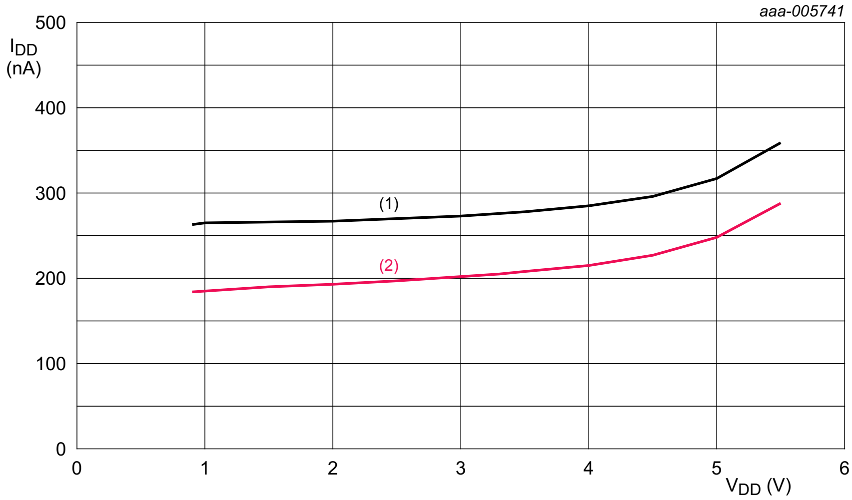
(2) V_{DD} = 3.3 V.

Fig 21. Typical I_{DD} as a function of temperature

T_{amb} = 25 °C; f_{CLKOUT} = 32768 Hz.

(1) 47 pF CLKOUT load.

(2) 22 pF CLKOUT load.

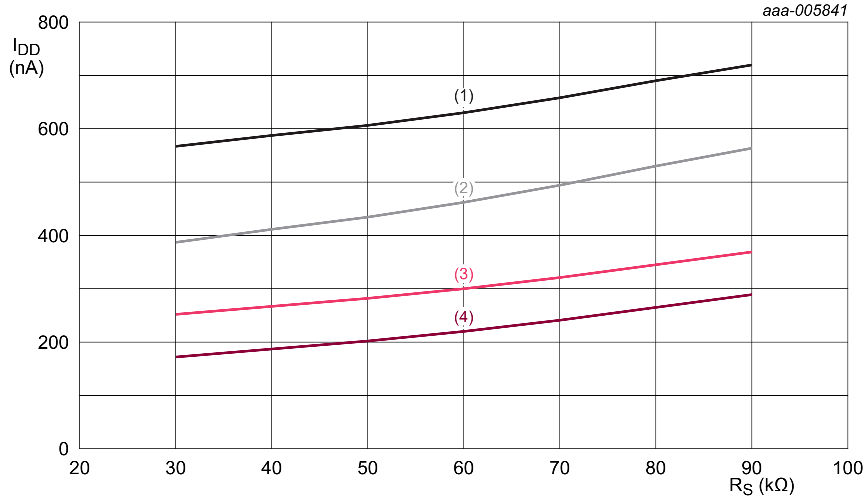


T_{amb} = 25 °C; CLKOUT disabled.

(1) $C_{L(itg)}$ = 12.5 pF.

(2) $C_{L(itg)}$ = 7 pF.

Fig 22. Typical I_{DD} with respect to V_{DD}



V_{DD} = 3.3 V; CLKOUT disabled.

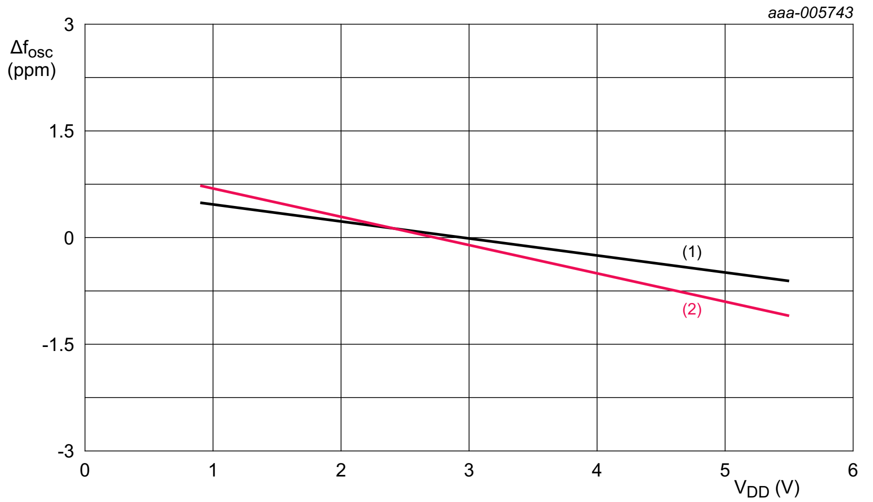
(1) $C_{L(itg)}$ = 12.5 pF; 50 °C; maximum value.

(2) $C_{L(itg)}$ = 7 pF; 50 °C; maximum value.

(3) $C_{L(itg)}$ = 12.5 pF; 25 °C; typical value.

(4) $C_{L(itg)}$ = 7 pF; 25 °C; typical value.

Fig 23. I_{DD} with respect to quartz R_S



T_{amb} = 25 °C.

(1) $C_{L(itg)}$ = 7 pF.

(2) $C_{L(itg)}$ = 12.5 pF.

Fig 24. Oscillator frequency variation with respect to V_{DD}

Table 32. I²C-bus characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 7 pF; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_b	capacitive load for each bus line		-	-	400	pF
f_{SCL}	SCL clock frequency	[2]	0	-	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
t_r	rise time of both SDA and SCL signals		20 + 0.1C_b	-	0.3	µs
t_f	fall time of both SDA and SCL signals		20 + 0.1C_b	-	0.3	µs
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
$t_{VD;DAT}$	data valid time		0	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time		0	-	0.9	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	-	50	ns

[1] A detailed description of the I²C-bus specification is given in Ref. 12 "UM10204".

[2] I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

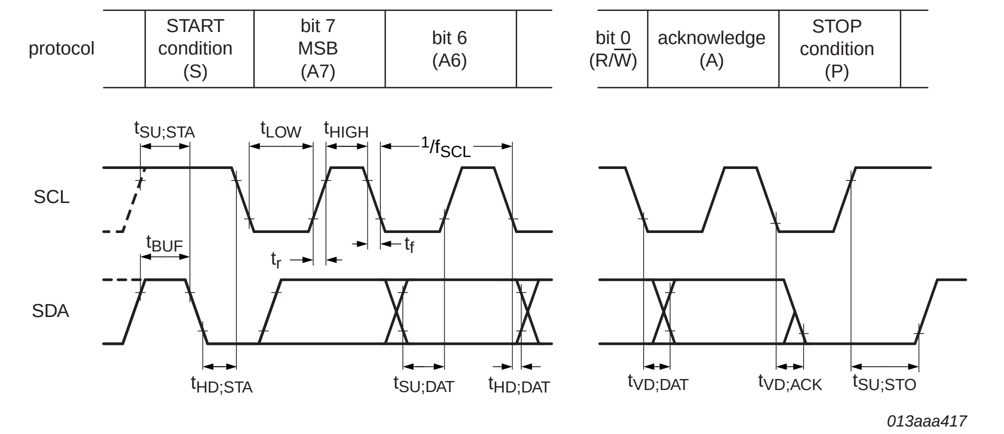
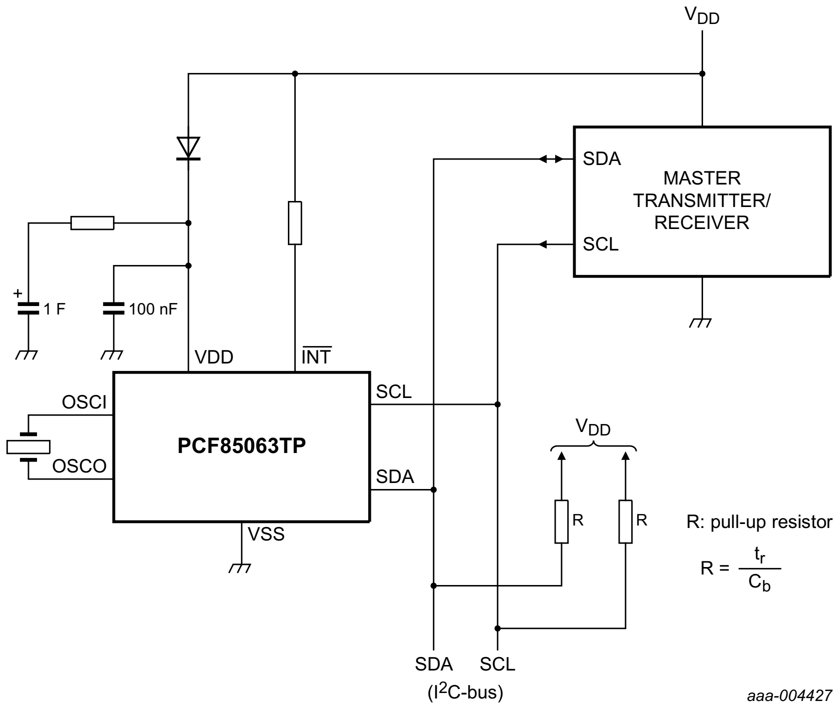


Fig 25. I²C-bus timing diagram; rise and fall times refer to 30 % and 70 %

13. Application information



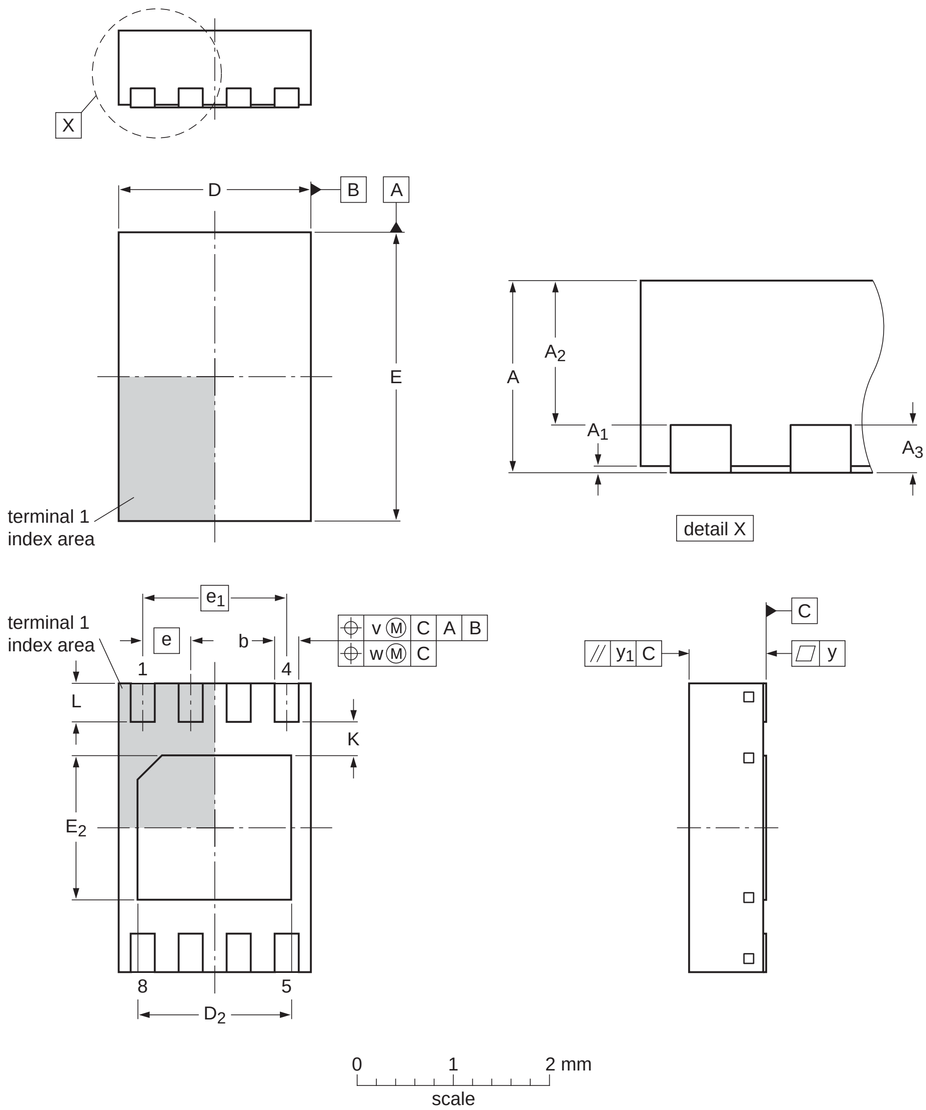
A 1 farad super capacitor combined with a low V_F diode can be used as a standby or back-up supply. With the RTC in its minimum power configuration i.e. timer off and CLKOUT off, the RTC may operate for weeks.

Fig 26. Application diagram for PCF85063TP

14. Package outline

HWSON8: plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 x 3 x 0.75 mm

SOT1069-2



Dimensions

Unit		A(1)	A_1	A_2	A_3	b	D(1)	D_2	E(1)	E_2	e	e_1	K	L	v	w	y	y_1
	max	0.80	0.05	0.65		0.30	2.1	1.6	3.1	1.6			0.40	0.45				
mm	nom	0.75	0.02	0.55	0.2	0.25	2.0	1.5	3.0	1.5	0.5	1.5	0.35	0.40	0.1	0.05	0.05	0.05
	min	0.70	0.00	0.45		0.18	1.9	1.4	2.9	1.4			0.30	0.35				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1069-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1069-2	- - -	MO-229	- - -			~~09-11-18~~ 12-04-18

Fig 27. Package outline SOT1069-2 (HWSON8) of PCF85063TP

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Packing information

16.1 Tape and reel information

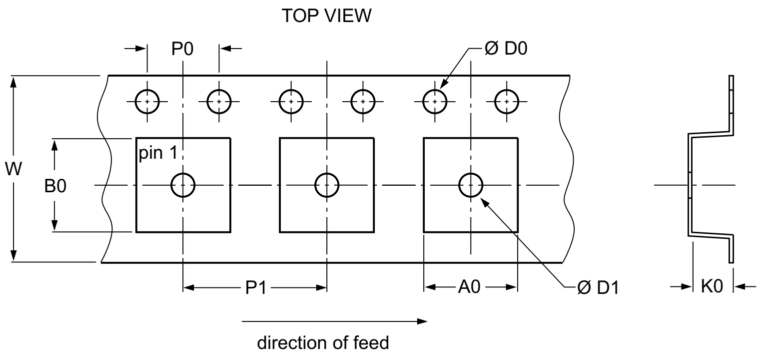


Fig 28. Tape and reel details for PCF85063TP

Table 33. Carrier tape dimensions of PCF85063TP
Nominal values without production tolerances.

Symbol	Description	Value	Unit
Compartments			
A0	pocket width in x direction	2.25	mm
B0	pocket width in y direction	3.25	mm
K0	pocket depth	1.05	mm
P1	pocket hole pitch	4	mm
D1	pocket hole diameter	1	mm
Overall dimensions			
W	tape width	8	mm
D0	sprocket hole diameter	1.55	mm
P0	sprocket hole pitch	4	mm

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 29) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 34 and 35

Table 34. SnPb eutectic process (from J-STD-020D)

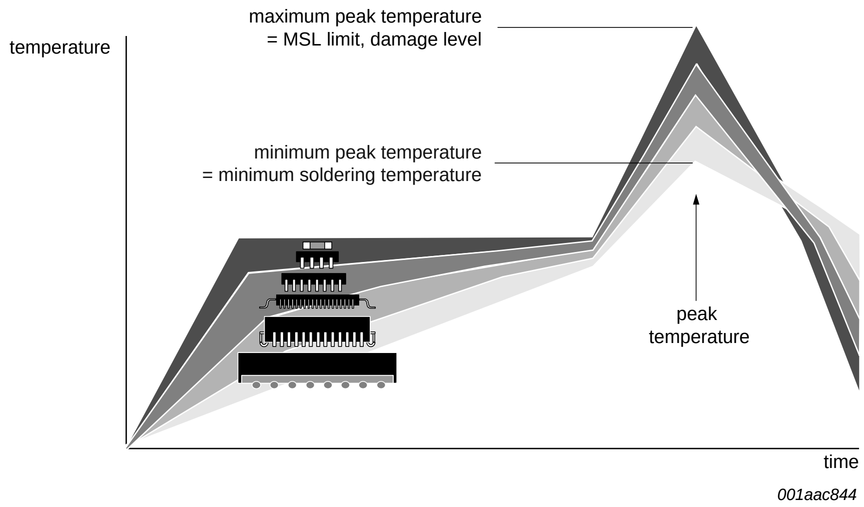
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 35. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 29.



MSL: Moisture Sensitivity Level

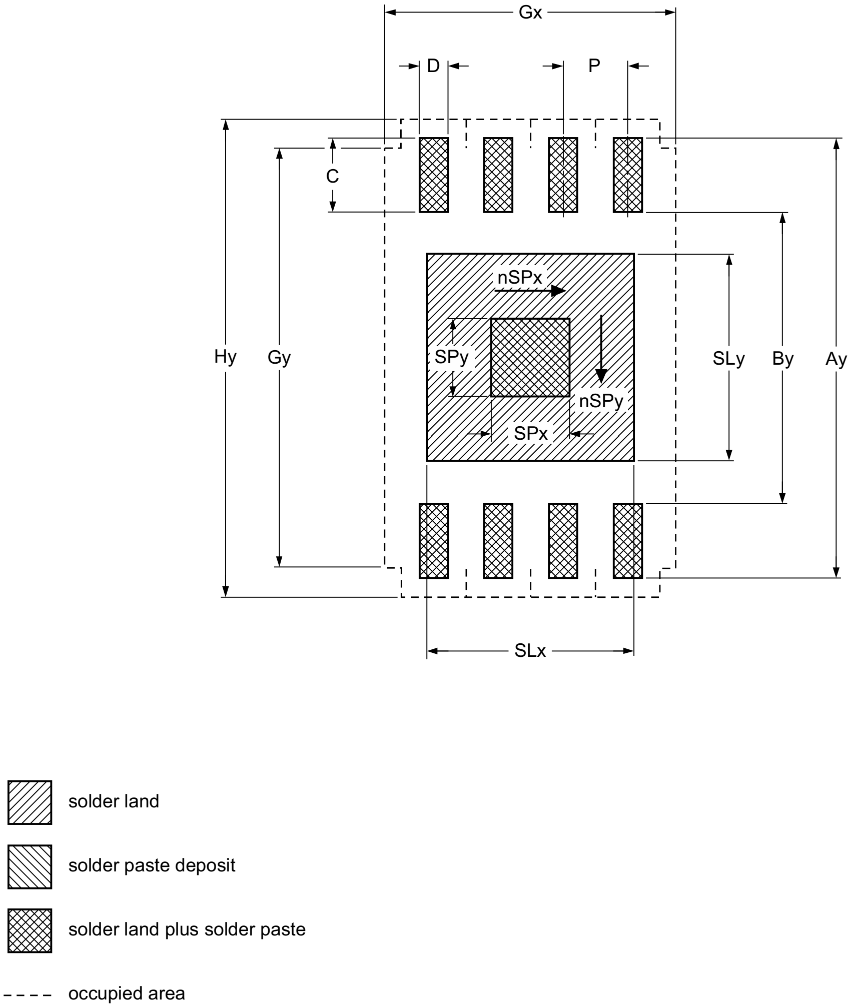
Fig 29. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

18. Footprint information

Footprint information for reflow soldering of HWSON8 package

SOT1069-2



DIMENSIONS in mm

P	Ay	By	C	D	SLx	SLy	SPx	SPy	Gx	Gy	Hy	nSPx	nSPy
0.5	3.45	2.2	0.625	0.25	1.6	1.6	0.6	0.6	2.25	3.25	3.7	1	1

Issue date ~~12-02-09~~ 12-02-22

sot1069-2_fr

Fig 30. Footprint information for reflow soldering of SOT1069-2 (HWSON8) of PCF85063TP

19. Abbreviations

Table 36. Abbreviations

Acronym	Description
BCD	Binary Coded Decimal
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RTC	Real-Time Clock
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface Mount Device

20. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10366 —** HVQFN application information

[3] **AN11247 —** Improved timekeeping accuracy with PCF85063, PCF8523 and PCF2123 using an external temperature sensor

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **IPC/JEDEC J-STD-020 —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[7] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[8] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[9] **JESD78 —** IC Latch-Up Test

[10] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[11] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[12] **UM10204 —** I^2C-bus specification and user manual

[13] **UM10569 —** Store and transport requirements

21. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF85063TP v.2	20130415	Product data sheet	-	PCF85063TP v.1
Modifications:	• Improved description of correction pulses (Table 14 and Table 16) • Adjusted I_{DD} and I_{LI} values (Table 31) • Updated Figure 19			
PCF85063TP v.1	20130122	Objective data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Tables

25. Figures

26. Contents

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